NEURAL INFORMATION PROCESSING SYSTEMS

LAMDA Learning And Mining from DatA

南京大学 NANJING UNIVERSITY 1902

Macro placement by wire-mask-guided black-box optimization

Yunqi Shi, Ke Xue, Lei Song, Chao Qian†
Email: qianc@lamda.nju.edu.cn

State Key Laboratory for Novel Software Technology
Nanjing University, Nanjing 210023, China

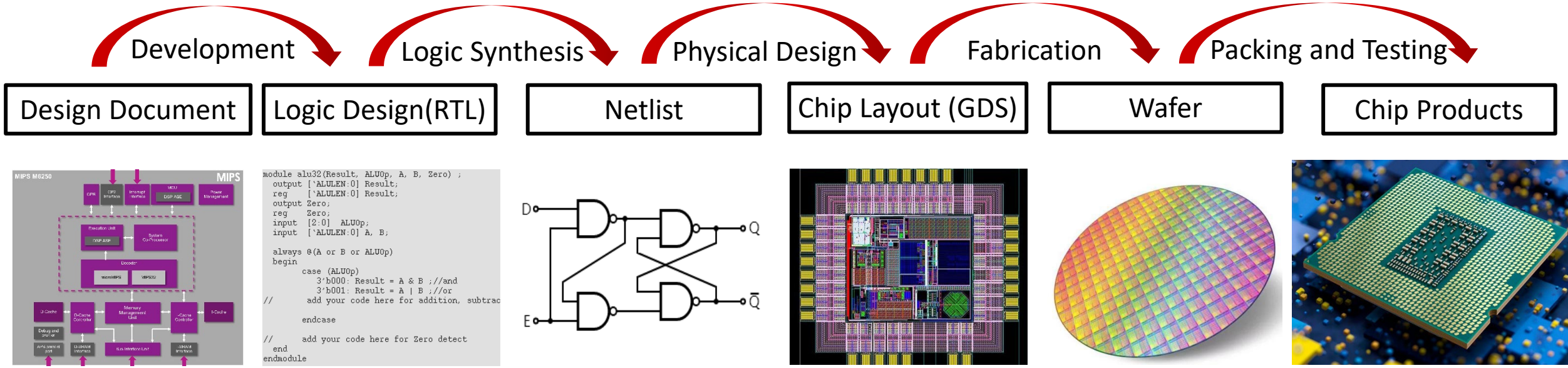
Electronic Design Automation (EDA)

Function design and verification: design the RTL and verify the functions. (Document -> RTL)

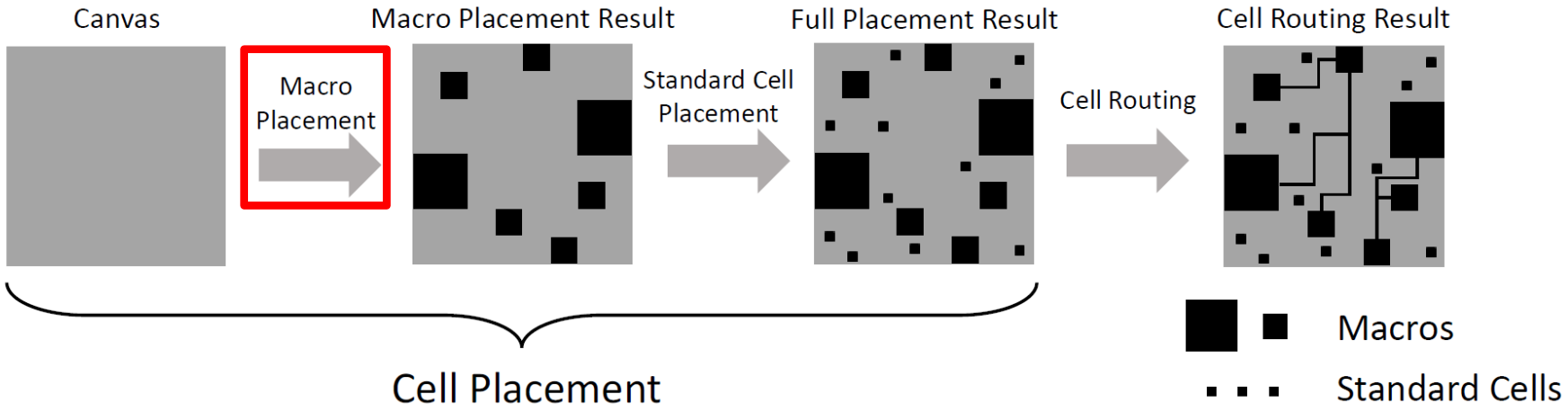
Logic synthesis: mapping the RTL design into netlist. (RTL -> Netlist)

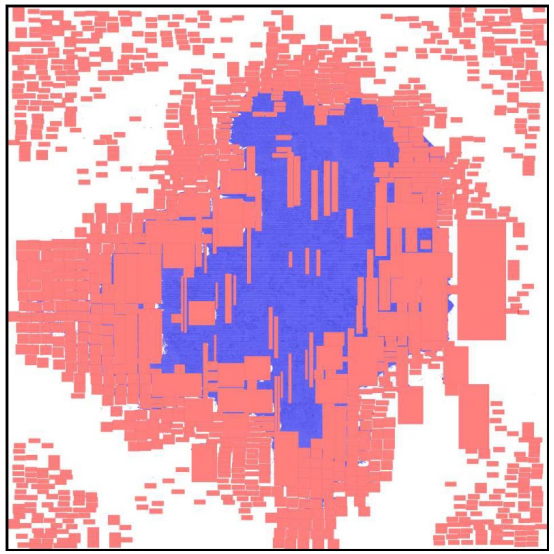
Physical design: design the physical layout according to netlist by EDA tools. (Netlist -> GDS)

Chip manufacturing: fabricate the chip from GDS layout by photolithography. (GDS -> Product)



Macro Placement





Objectives: HPWL, congestion, density……

Constraint: non-overlapping

#number of macros: thousands

Black-box, Multi-objective

Hard constraint

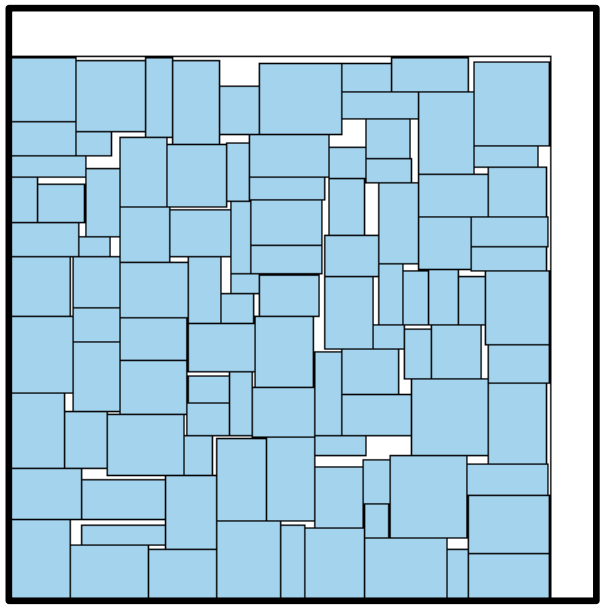
High-dimension

} **Challenges**

Motivation

Problems of the existing methods:

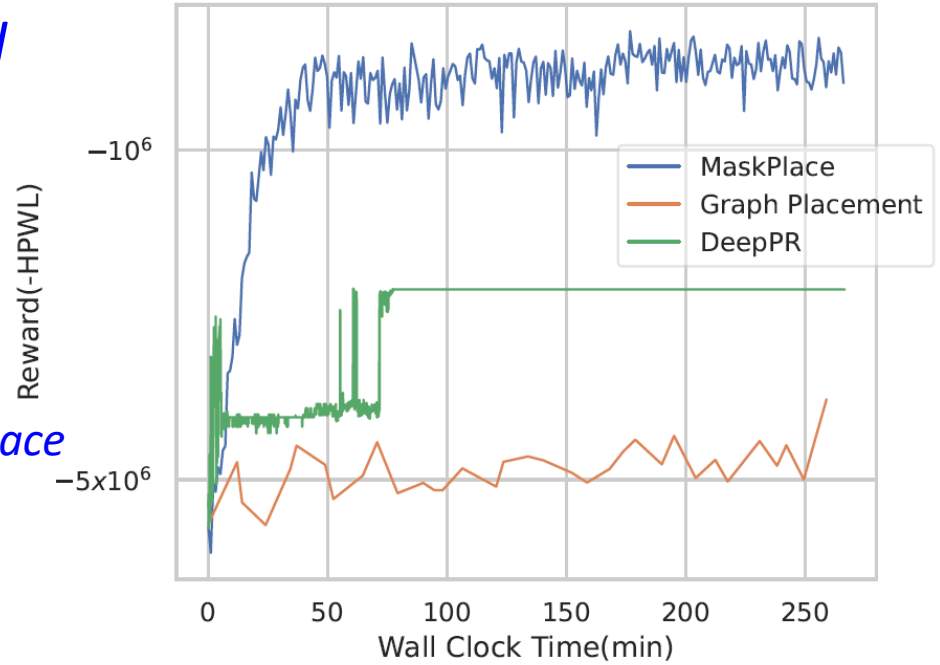
- Packing-based methods *hardly handle standard cells, low efficiency*
- Analytical placer *objective definition, overlapping*
- Reinforcement placer (MaskPlace) *under-explored*



A packing placement solution

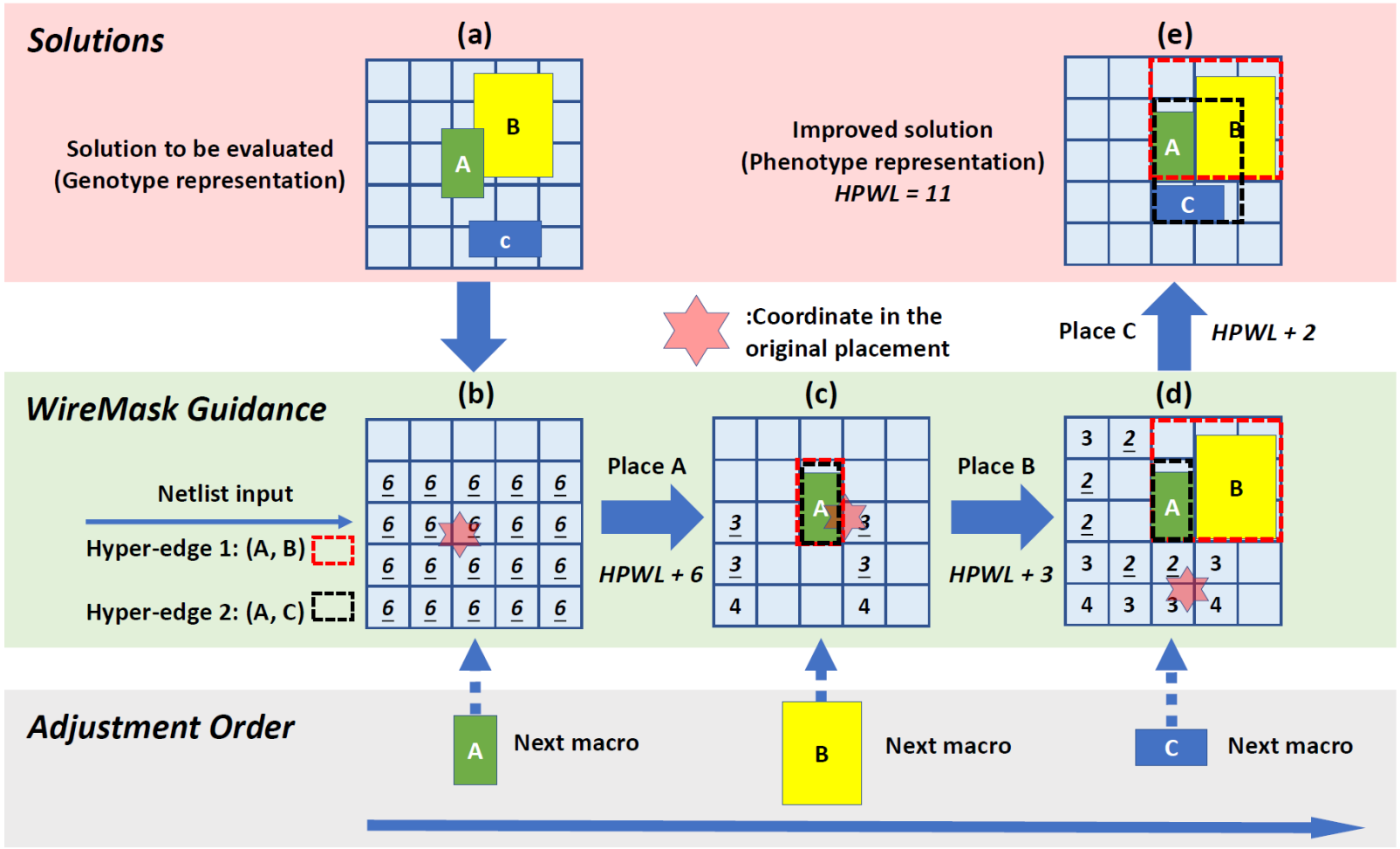
Converge in less than 1 hour,

Too fast compared to a large search space



Converging curve of MaskPlace

WireMask-BBO Framework



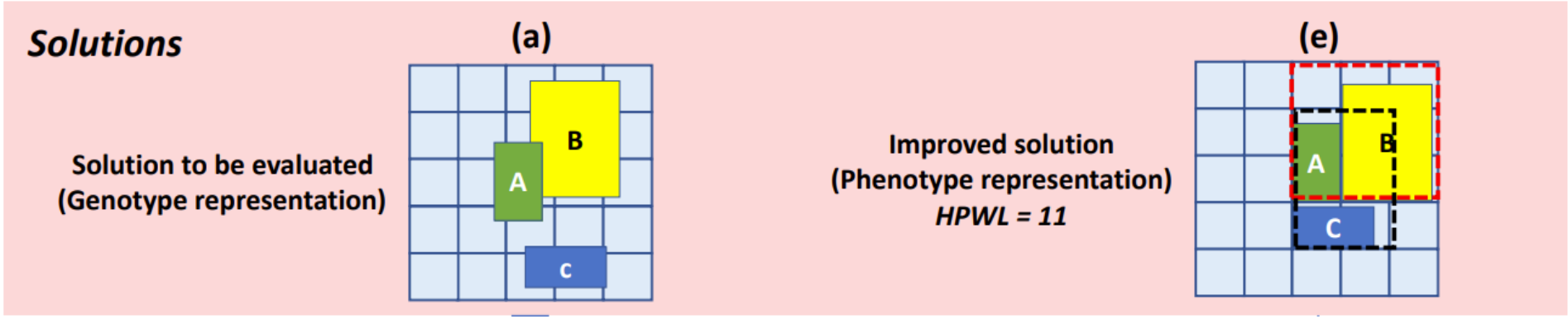
Improve efficiency
Keep non-overlapping
Ensure quality

Any black-box optimization algorithm

Good exploration

Greedy improvement guided by wire mask

WireMask-BBO Framework



We can modify the solution **without concerning the constraint of overlap**.

How to optimize? Random Search / Evolutionary Algorithm / Bayesian Optimization

- RS: randomly decide the coordinate of the macros
- EA: exchange 2 randomly selected macros
- BO: optimize the coordinate of the macros directly

Experiments

Comparison with state-of-the-art methods

Table 1: HPWL values ($\times 10\text{^}5$) obtained by ten compared methods on seven chips. Each result consists of the mean and standard deviation of five runs. The best (smallest) mean value on each chip is bolded.

	Method	Type	adaptec1	adaptec2	adaptec3	adaptec4	bigblue1	bigblue3	bigblue4 ($\times 10^7$)	+/ − / ≈	Avg. Rank
Packing-based method	SP-SA [33]	Packing	18.84 ± 4.62	117.36 ± 8.73	115.48 ± 7.56	120.03 ± 4.25	5.12 ± 1.43	164.70 ± 19.55	25.49 ± 2.73	0/7/0	6.86
Analytical	NTUPlace3 [12]	Analytical	26.62	321.17	328.44	462.93	22.85	455.53	48.38	0/7/0	9.00
Analytical	RePlace [13]	Analytical	16.19 ± 2.10	153.26 ± 29.01	111.21 ± 11.69	37.64 ± 1.05	2.45 ± 0.06	119.84 ± 34.43	11.80 ± 0.73	1/6/0	5.28
Analytical	DREAMPlace [28]	Analytical	15.81 ± 1.64	140.79 ± 26.73	121.94 ± 25.05	**37.41 ± 0.87**	2.44 ± 0.06	107.19 ± 29.91	12.29 ± 1.64	1/6/0	4.86
RL	Graph [32]	RL	30.10 ± 2.98	351.71 ± 38.20	358.18 ± 13.95	151.42 ± 9.72	10.58 ± 1.29	357.48 ± 47.83	53.35 ± 4.06	0/7/0	9.00
RL	DeepPR [15]	RL	19.91 ± 2.13	203.51 ± 6.27	347.16 ± 4.32	311.86 ± 56.74	23.33 ± 3.65	430.48 ± 12.18	68.30 ± 4.44	0/7/0	8.86
RL	MaskPlace [26]	RL	6.38 ± 0.35	73.75 ± 6.35	84.44 ± 3.60	79.21 ± 0.65	2.39 ± 0.05	91.11 ± 7.83	11.07 ± 0.90	0/7/0	4.28
Our methods	WireMask-RS	Ours	6.13 ± 0.05	59.28 ± 1.48	60.60 ± 0.45	62.06 ± 0.22	2.19 ± 0.01	62.58 ± 2.07	**8.20 ± 0.17**	0/5/2	2.57
Our methods	WireMask-BO	Ours	6.07 ± 0.14	59.17 ± 3.94	61.00 ± 2.08	63.86 ± 1.01	2.14 ± 0.03	67.48 ± 6.49	8.62 ± 0.18	0/3/4	2.86
Our methods	WireMask-EA	Ours	**5.91 ± 0.07**	**52.63 ± 2.23**	**57.75 ± 1.16**	58.79 ± 1.02	**2.12 ± 0.01**	**59.87 ± 3.40**	8.28 ± 0.25	–	**1.43**

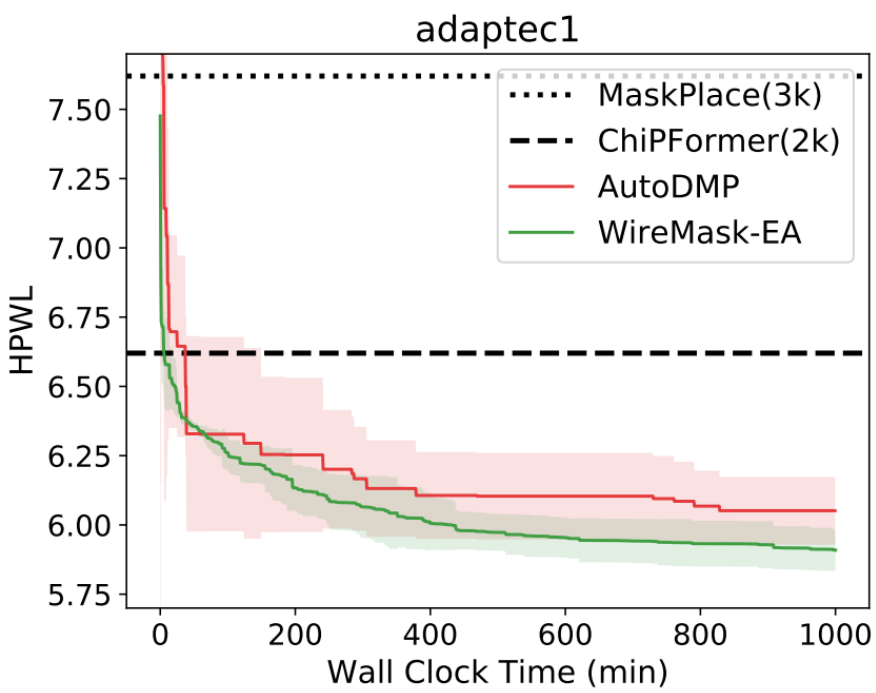
Nature 2021

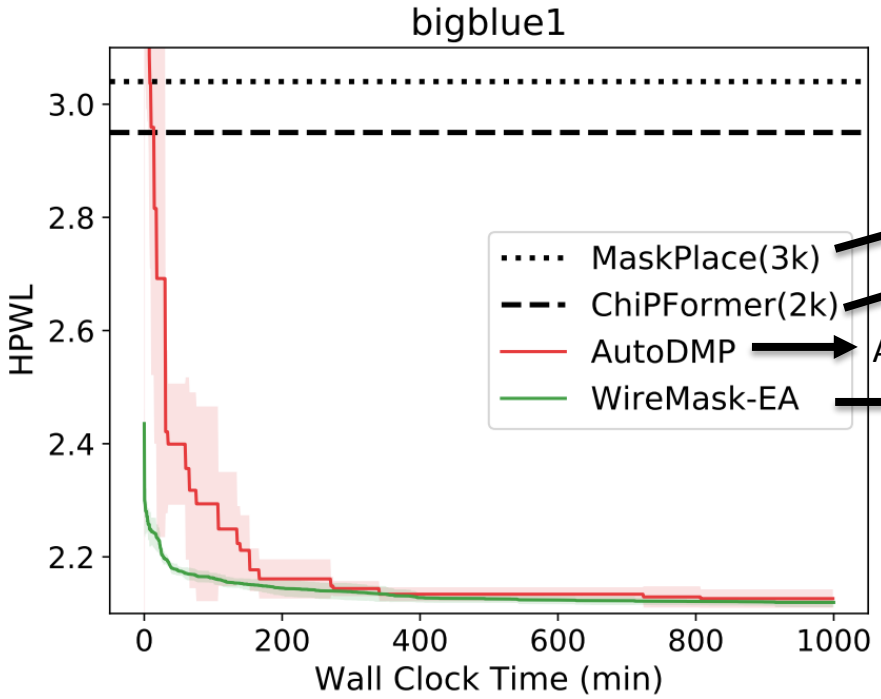
WireMask-EA achieves the best average rank, and performs the best on 5 out of 7 chips.

WireMask-EA is significantly better than any previous method on at least 6 out of the 7 chips.

Experiments

Comparison on wall clock time





RL method, NeurIPS'22

RL method, ICML'23

Analytical method, ISPD'23

Our method

WireMask-EA is better than two concurrent state-of-the-art methods

Experiments

Fine-tune existing placement

Table 5: HPWL (×10^5) values obtained after fine-tuning existing placements by running WireMaskEA for 1,000 minutes.

Method	adaptec1	adaptec2	adaptec3	adaptec4	bigblue1	bigblue3	Avg. Imp.
SP-SA [33]	18.84	117.36	115.48	120.03	5.12	164.70	53.93%
+WireMask-EA (1000min)	6.02 ± 0.11	60.35 ± 4.41	57.88 ± 0.62	59.50 ± 0.92	2.21 ± 0.02	82.68 ± 18.17	
MaskPlace [26]	6.56	79.98	79.32	75.75	2.42	82.61	17.06%
+WireMask-EA (1000min)	5.84 ± 0.10	61.43 ± 1.23	59.24 ± 2.71	60.35 ± 1.38	2.10 ± 0.01	74.93 ± 7.79	

WireMask-EA takes any existing placement as the initial solution, and further optimize it.

The fine-tuning result of state-of-the-art method MaskPlace shows significant improvement.

Discussion

Conclusion

- A general framework **WireMask-BBO** is proposed for solving macro placement task and can be equipped with **any BBO algorithms**.
- Experiments show the **superior performance** of WireMask-BBO over previous packing-based, analytical and RL-based methods.
- WireMask-BBO can be combined with any existing macro placement methods to **fine-tune and further improve** the placement result.

Limitations

- It can only deal with macro placement, leaving standard cells for analytical placers.
- The performance is limited for chips with large number of macros (e.g. bigblue4 with over 8,000 macros), due to expensive objective evaluation.

Thank you for your listening!